CLAIMS

1. An amplifier circuit comprising:

a first input terminal;

a second input terminal;

a first output terminal;

a second output terminal;

a first complementary metal-oxide-semiconductor (CMOS) inverter coupled between the first input terminal and the first output terminal;

a first bias circuit for applying linear biasing to the first CMOS inverter, the first bias circuit being coupled between an output of the first CMOS inverter and the input of the first CMOS inverter;

a second CMOS inverter coupled between the second input terminal and the second output terminal; and

a second bias circuit for applying linear biasing to the second CMOS inverter, the second bias circuit being coupled between an output of the second CMOS inverter and the input of the second CMOS inverter.

2. The amplifier circuit of Claim 1, wherein the first input terminal is coupled to the input of the first CMOS inverter by a first capacitor, and

wherein the second input terminal is coupled to the input of the second CMOS inverter by a second capacitor.

3. The amplifier circuit of Claim 1, wherein the first CMOS inverter comprises a first p-type metal-oxide-semiconductor (PMOS) transistor and a first n-type metal-oxide-semiconductor (NMOS) transistor,

wherein the second CMOS inverter comprises a second PMOS transistor and a second NMOS transistor,

wherein the first PMOS transistor and the first NMOS transistor are serially connected between an upper supply voltage and a lower supply voltage,

wherein the second PMOS transistor and the second NMOS transistor are serially connected between the upper supply voltage and the lower supply voltage,

wherein a gate of the first PMOS transistor and a gate of the first NMOS transistor are connected to the input of the first CMOS inverter,

wherein a gate of the second PMOS transistor and a gate of the second NMOS transistor are connected to the input of the second CMOS inverter,

wherein a drain of the first PMOS transistor and a drain of the first NMOS transistor are connected to the output of the first CMOS inverter, and

wherein a drain of the second PMOS transistor and a drain of the second NMOS transistor are connected to the output of the second CMOS inverter.

4. The amplifier circuit of Claim 3, wherein the first bias circuit comprises a first operational amplifier (op-amp), a non-inverting input of the first op-amp being coupled to the output of the first CMOS inverter, an output of the first op-amp being coupled to the input of the first CMOS inverter, and an inverting input of the first op-amp being coupled to receive a reference voltage, the reference voltage being between the first supply voltage and the second supply voltage, and the first supply voltage being greater than the second supply voltage, and

wherein the second bias circuit comprises a second op-amp, a non-inverting input of the second op-amp being coupled to the output of the second CMOS inverter, an output of the second op-amp being coupled to the input of the second CMOS inverter, and

an inverting input of the second op-amp being coupled to receive the reference voltage.

5. The amplifier circuit of Claim 4, wherein the reference voltage is halfway between the first supply voltage and the second supply voltage.

6. The amplifier circuit of Claim 4, wherein the non-inverting input of the first op-amp is coupled to the output of the first CMOS inverter by a first resistor,

wherein the output of the first op-amp is coupled to the input of the first CMOS inverter by a second resistor,

wherein the non-inverting input of the second op-amp is coupled to the output of the second CMOS inverter by a third resistor, and

wherein the output of the second op-amp is coupled to the input of the second CMOS inverter by a fourth resistor.

7. The amplifier circuit of Claim 6, wherein the non-inverting input of the first op-amp is coupled to the second supply voltage by a first capacitor,

wherein the output of the first op-amp is coupled to the second supply voltage by a second capacitor,

wherein the non-inverting input of the second op-amp is coupled to the second supply voltage by a third capacitor, and

wherein the output of the second op-amp is coupled to the second supply voltage by a fourth capacitor.

8. The amplifier circuit of Claim 1, further comprising:

a first amplifier stage coupled to the first output terminal; and

a second amplifier stage coupled to the second output terminal.

9. The amplifier circuit of Claim 8, wherein the first amplifier stage comprises a third input terminal coupled to the first output terminal, a third output terminal, a third CMOS inverter coupled between the third input terminal and the third output terminal, and a third bias circuit for applying linear biasing to the third CMOS inverter, the third bias circuit being coupled between an output of the third CMOS inverter and the input of the third CMOS inverter, and

wherein the second amplifier stage comprises a fourth input terminal coupled to the first output terminal, a fourth output terminal, a fourth CMOS inverter coupled between the fourth input terminal and the fourth output terminal, and a fourth bias circuit for applying linear biasing to the fourth CMOS inverter, the fourth bias circuit being coupled between an output of the fourth CMOS inverter and the input of the fourth CMOS inverter.

10. A method for operating a high frequency amplifier, the method comprising:

providing a first complementary metal-oxide-semiconductor (CMOS) inverter and a second CMOS inverter;

applying linear biasing to the first CMOS inverter and the second CMOS inverter;

supplying a first alternating current (AC) signal to the input of the first CMOS inverter and a second AC signal to the input of the second CMOS inverter to generate an amplified differential signal.

11. The method of Claim 10, wherein applying linear biasing to the first CMOS inverter comprises supplying a DC bias

voltage to the input of the first CMOS inverter to drive a first DC offset voltage at an output of the first CMOS inverter to a reference voltage, and

wherein applying linear biasing to the second CMOS inverter comprises supplying the DC bias voltage to the input of the second CMOS inverter to drive a second DC offset voltage at an output of the second CMOS inverter to the reference voltage.

12. The method of Claim 11, wherein supplying the DC offset voltage to the input of the first CMOS inverter comprises providing the DC offset voltage to a non-inverting input of a first operational amplifier (op-amp), providing the reference voltage to an inverting input of the first op-amp, and providing an output voltage of the first op-amp to the input of the first CMOS inverter, and

wherein supplying the DC offset voltage to the input of the second CMOS inverter comprises providing the DC offset voltage to a non-inverting input of a second op-amp, providing the reference voltage to an inverting input of the second op-amp, and providing an output voltage of the second op-amp to the input of the second CMOS inverter.

13. The method of Claim 12, wherein providing the DC offset voltage to the non-inverting input of the first op-amp comprises coupling the output of the first CMOS inverter to the non-inverting input of the first op-amp via a first resistor,

wherein providing the output voltage of the first op-amp to the input of the first CMOS inverter comprises coupling an output of the first op-amp to the input of the first CMOS inverter via a second resistor,

wherein providing the DC offset voltage to the non-inverting input of the second op-amp comprises coupling the

output of the second CMOS inverter to the non-inverting input of the second op-amp via a third resistor, and

wherein providing the output voltage of the second op-amp to the input of the second CMOS inverter comprises coupling an output of the second op-amp to the input of the second CMOS inverter via a fourth resistor.

14. The method of Claim 13, wherein the first CMOS inverter comprises a first PMOS transistor and a first NMOS transistor serially connected between an upper supply voltage and a lower supply voltage,

wherein the second CMOS inverter comprises a second PMOS transistor and a second NMOS transistor serially connected between the upper supply voltage and the lower supply voltage, and

wherein the reference voltage is halfway between the upper supply voltage and the lower supply voltage.

15. The method of Claim 14, wherein providing the output voltage of the first op-amp to the input of the first CMOS inverter further comprises coupling the output of the first op-amp to the lower supply voltage via a first capacitor,

wherein providing the DC offset voltage to the non-inverting input of the first op-amp further comprises coupling the non-inverting input of the first op-amp to the lower supply voltage via a second capacitor,

wherein providing the output voltage of the second op-amp to the input of the second CMOS inverter further comprises coupling the output of the second op-amp to the lower supply voltage via a third capacitor, and

wherein providing the DC offset voltage to the non-inverting input of the second op-amp further comprises coupling

the non-inverting input of the second op-amp to the lower supply voltage via a fourth capacitor.

16. The method of Claim 14, wherein supplying a first alternating current (AC) signal to the input of the first CMOS inverter and a second AC signal to the input of the second CMOS inverter comprises:

receiving a first high frequency input signal;

filtering out DC components from the first high frequency input signal to generate the first AC signal;

receiving a second high frequency input signal; and

filtering out DC components from the second high frequency input signal to generate the second AC signal.

17. A high frequency amplifier comprising:

a first complementary metal-oxide-semiconductor (CMOS) inverter;

a second CMOS inverter;

means for regulating a first DC bias voltage at an input of the first CMOS inverter to force a DC offset voltage at an output of the first CMOS inverter to a reference voltage between an upper supply voltage and a lower supply voltage; and

means for regulating a second DC bias voltage at an input of the second CMOS inverter to force a DC offset voltage at an output of the second CMOS inverter to the reference voltage.

18. The high frequency amplifier of Claim 17, wherein the first CMOS inverter comprises a first p-type metal-oxide-semiconductor (PMOS) transistor and a first n-type metal-oxide-

semiconductor (NMOS) transistor serially connected between an upper supply voltage and a lower supply voltage,

wherein the second CMOS inverter comprises a second PMOS transistor and a second NMOS transistor serially connected between the upper supply voltage and the lower supply voltage, the reference voltage being between the upper supply voltage and the lower supply voltage.

19. The high frequency amplifier of Claim 18, wherein the reference voltage is halfway between the upper supply voltage and the lower supply voltage.

20. The high frequency amplifier of Claim 18, wherein the means for regulating the first DC bias voltage comprises a first operational amplifier (op-amp), a non-inverting input of the first op-amp being coupled to the output of the CMOS inverter via a first resistor, an inverting input of the first op-amp being coupled to receive the reference voltage, and an output of the first op-amp being coupled to the input of the first CMOS inverter via a second resistor, and

wherein the means for regulating the second DC bias voltage comprises a second op-amp, a non-inverting input of the second op-amp being coupled to the output of the CMOS inverter via a third resistor, an inverting input of the second op-amp being coupled to receive the reference voltage, and an output of the second op-amp being coupled to the input of the second CMOS inverter via a fourth resistor

21. The high frequency amplifier of Claim 22, wherein the means for regulating the first DC bias voltage further comprises a first capacitor coupled between the non-inverting input of the first op-amp and the lower supply voltage, and a second

capacitor coupled between the output of the first op-amp and the lower supply voltage, and

wherein the means for regulating the second DC bias voltage further comprises a third capacitor coupled between the non-inverting input of the second op-amp and the lower supply voltage, and a fourth capacitor coupled between the output of the second op-amp and the lower supply voltage

22. An amplification circuit comprising:

a first complementary metal-oxide-semiconductor (CMOS) inverter coupled between an upper supply voltage and a lower supply voltage;

a second CMOS inverter coupled between the upper supply voltage and the lower supply voltage;

a first operational amplifier (op-amp), a non-inverting input of the first op-amp being coupled to an output of the first CMOS inverter, an inverting input of the first op-amp being coupled to receive a reference voltage, the reference voltage being between the upper supply voltage and the lower supply voltage, and an output of the first op-amp being coupled to an input of the first CMOS inverter; and

a second op-amp, a non-inverting input of the second op-amp being coupled to an output of the second CMOS inverter, an inverting input of the second op-amp being coupled to receive the reference voltage, and an output of the second op-amp being coupled to an input of the second CMOS inverter.

23. The amplification circuit of Claim 22, wherein the non-inverting input of the first op-amp is coupled to the output of the first CMOS inverter by a first resistor,

wherein the output of the first op-amp is coupled to the input of the first CMOS inverter by a second resistor,

wherein the non-inverting input of the second op-amp is coupled to the output of the second CMOS inverter by a third resistor, and

wherein the output of the second op-amp is coupled to the input of the second CMOS inverter by a fourth resistor.

24. The amplification circuit of Claim 23, wherein the non-inverting input of the first op-amp is coupled to the lower supply voltage by a first capacitor,

wherein the output of the first op-amp is coupled to the lower supply voltage by a second capacitor,

wherein the non-inverting input of the second op-amp is coupled to the lower supply voltage by a third capacitor, and

wherein the output of the second op-amp is coupled to the lower supply voltage by a fourth capacitor.

25. The amplification circuit of Claim 24, further comprising:

a first input terminal coupled to the input of the first CMOS inverter by a fifth capacitor; and

a second input terminal coupled to the input of the second CMOS inverter by a sixth capacitor.